LISTING OF THE CLAIMS:

The following is a complete listing of all the claims in the application, with an indication of the status of each:

1. (Currently Amended) An electronic circuit for cryptographic processing, ~~having a set of combinatorial logical circuits, the set of combinatorial logical circuits~~ comprising:

a first combinatorial logical circuit, having an input, arranged to perform a first set of logical operations on an input data at the input and to produce a corresponding first output data, the first output data having a first functional relation to the input data for said input data within a given range, and ~~characterized in that the set of combinatorial logical circuits further comprises at least~~

a second combinatorial logical circuit, having an input, arranged to perform a second set of logical operations on an ~~the same~~ input data at said input and to produce a corresponding second output data, the second output data having a second ~~an identical~~ functional relation to the input data, said second functional relation identical to said first functional relation for said input data within said given range,

wherein the first set of logical operations is different from the second set of logical operations, and a selector for receiving a given input data and ~~wherein the electronic circuit is arranged to~~ dynamically selecting from among the first ~~one~~ combinatorial logical circuit for performing the first set of logical operations on the given input data and the second combinatorial logical circuit ~~of the set of combinatorial logical circuits~~ for performing the second set of logical operations on the given ~~the~~ input data and producing output data, and

wherein the selecting includes inputting the given input data to the input of the selected one of the first and second combinatorial logical circuits and outputting a selected first cryptographic processing output, the selected first cryptographic processing output being the output of the selected one of the first and second combinatorial logical circuits.

2. (Currently Amended) The ~~An~~ electronic circuit of ~~according to~~ claim 1, further comprising:

a third combinatorial logical circuit, having an input, arranged to perform a third set of logical operations on an input data at said input and to produce a corresponding third output data, the third output data having a third given functional relation to said input data for input data within a given range, and

a fourth combinatorial logical circuit, having an input, arranged to perform a fourth set of logical operations on an input data at said input and to produce a corresponding fourth output data, the fourth output data having a fourth functional relation to said input data identical to said given third functional relation,

wherein the third set of logical operations is different from the fourth set of logical operations, and

a selector for receiving said selected first cryptographic processing output data and dynamically selecting from among the third combinatorial logical circuit and the fourth combinatorial logical circuit for performing logical operations on the selected first cryptographic processing output data and producing a second output cryptographic processing data, and

wherein said selecting includes inputting the selected first cryptographic processing output data to the input of the selected one of the third and fourth combinatorial logical circuits ~~comprising at least a first set of combinatorial logical circuits and a second set of combinatorial logical circuits, and arranged to use output data produced by the first set of combinatorial logical circuits as input data of the second set of combinatorial logical circuits~~.

3. (Currently Amended) The ~~An~~ electronic circuit of ~~according to~~ claim 1, wherein the selector comprises ~~further comprising~~:

[[-]] a selection circuit ~~arranged~~ for generating a selecting signal to select one combinatorial logical circuit from among ~~of~~ the first and second ~~set of~~ combinatorial logical circuits,

[[-]] a splitter circuit ~~arranged~~ for inputting the given input data to one of the first and second combinatorial logical ~~circuit of the set of combinatorial logical~~ circuits, depending on the selecting signal,

[[-]] a merger circuit ~~arranged~~ for outputting data from one of the first and second combinatorial logical ~~circuit of the set of combinatorial logical~~ circuits, depending on the selecting signal.

4. (Currently Amended) The ~~An~~ electronic circuit of ~~according to~~ claim 3, further comprising a timing circuit ~~arranged~~ to determine the points in time at which the selection circuit generates the selecting signal to select one of the first and second combinatorial logical combinatorial logical ~~circuit of the set of combinatorial logical~~ circuits.

5. (Currently Amended) An electronic circuit for cryptographic processing, comprising:

[[-]] a combinatorial logical circuit ~~arranged~~ to perform logical operations on input data and to produce an output data,

[[-]] a storage circuit ~~element~~ for storing the output data produced by the combinatorial logical circuit, ~~characterized in that~~

wherein the storage ~~electronic~~ circuit ~~further~~ comprises

a first ~~set of an~~ encoding means for encoding the output data into a first encoded output data, a storage element for retrievably storing the first encoded output data,

a corresponding first decoding means, arranged for ~~encoding output data before storing the first output data in the storage element and~~ decoding the first encoded output data into said output data after retrieving the first encoded output data from the storage element~~, respectively~~, and

wherein the electronic circuit is arranged to dynamically control the activation of the first ~~set of an~~ encoding means and the [[a]] corresponding first decoding means.

6. (Currently Amended) The ~~An~~ electronic circuit of ~~according to~~ claim 5, wherein the storage circuit further comprises ~~comprising:~~

a second ~~set of an~~ encoding means for encoding the output data into a second encoded output data for storing in the storage element,

a corresponding second decoding means, arranged for ~~encoding output data before storing the first output data in the storage element and~~ decoding the second encoded output data into said output data after retrieving the second encoded output data from the storage element~~, respectively~~,

wherein the encoding of the first output data is different from the encoding of the second output data, and

wherein the electronic circuit is further arranged to generate a selecting signal to dynamically select from among the first ~~one set of an~~ encoding means and its [[a]] corresponding first decoding means and the second ~~set of an~~ encoding means and its [[a]] corresponding second decoding means, for encoding and decoding of the output data.

7. (Currently Amended) The ~~An~~ electronic circuit of ~~according to~~ claim 6, further comprising a timing circuit ~~arranged~~ to determine the points in time at which the electronic circuit selects one from among the first and second ~~set of~~ encoding means and corresponding first and second decoding means~~, of a set comprising at least the first set of an encoding means and a corresponding decoding means and the second set of encoding means and a corresponding decoding means~~..

8. (Currently Amended) The ~~An~~ electronic circuit of ~~according to~~ claim 6 [[5]], wherein the combinatorial logical circuit comprises:

a first combinatorial logical circuit, having an input, arranged to perform a first set of logical operations on input data at the input and to produce a corresponding first cryptographic output data, the first cryptographic output data having a given first functional relation to the input data for said input data within a given range, and ~~characterized in that the set of combinatorial logical circuits further comprises at least~~

a second combinatorial logical circuit, having an input, arranged to perform a second set of logical operations on ~~the same~~ input data at said input and to produce a corresponding second cryptographic output data, the second cryptographic output data having a ~~an identical~~ functional relation to the input data identical to the given first functional relation for said input data within said given range,

wherein the first set of logical operations is different from the second set of logical operations, and

a selector for receiving an input data and ~~wherein the electronic circuit is arranged to~~ dynamically selecting from among the first ~~one~~ combinatorial logical circuit and the second combinatorial logical circuit ~~of the set of combinatorial logical circuits~~ for performing logical operations on the given ~~the~~ input data and producing output data, and

wherein the selecting includes inputting the input data to the input of the selected one of the first and second combinatorial logical circuits and outputting a selected output, the selected output being the output of the selected one of the first and second combinatorial logical circuits.

9. (Canceled)

10. (Currently Amended) A method of processing cryptographic data, comprising:

[[-]] using a set of logical operations for processing input data and producing output data,

[[-]] storing the output data in a storage element, wherein the storing ~~characterized in that the method further~~ comprises:

[[-]] encoding the output data into an encoded output data ~~before storing the output data in the storage element~~,

storing the encoded output data in the storage element,

retrieving the encoded output data from the storage element,

[[-]] decoding the encoded output data retrieved ~~after retrieving~~ from the storage element, and

dynamically controlling the encoding of the output data into an encoded output data and the corresponding decoding of the encoded output data retrieved from the storage element.

11. (Original) A cryptographic device comprising an electronic circuit according to claim 1.

12. (New) The electronic circuit of claim 1, wherein the selector includes:

a first mask circuit for selectively masking and not masking, based on the signal, the given input data for input to the first combinatorial logical circuit, and

a second mask circuit for selectively masking and not masking, based on the signal, the given input data for input to the second combinatorial logical circuit.

13. (New) The electronic circuit of claim 8, wherein the selector includes:

a first mask circuit to selectively mask and not mask, based on the signal, the given input data and to input the selected masked and not masked given input data to the first combinatorial logical circuit, and

a second mask circuit to selectively mask and not mask, based on the signal, to input the selected masked and not masked given input data to the second combinatorial logical circuit.

14. (New) The electronic circuit of claim 13,

wherein the first mask circuit includes an AND mask configured to mask and to not mask the given input data by inputting to the first combinatorial logical circuit a selection between all zeros and the given input data, respectively and

wherein the second mask circuit includes an AND mask configured to mask and to not mask the given input data by inputting to the second combinatorial logical circuit a selection between all zeros and the given input data, respectively.

15. (New) The electronic circuit of claim 1, wherein the selector includes an OR merger circuit to receive the output of the first combinatorial logical circuit and to receive the output of the second combinatorial logic circuit, and to output, as the selected output, a logical OR of the output of the first

combinatorial logical circuit and the output of the second combinatorial logic circuit.

16. (New) A method of processing cryptographic data, comprising:

generating a mode signal having one of a given plurality of states;

receiving a given input data and generating a cryptographic processed data output, said generating including:

generating a first input data, wherein the first input data is a selected one of a mask of the given input data and a not mask of the given data, the selection based on the state of the mode signal;

generating a second input data, wherein the second input data is the other of the mask of the given input data and the not mask of the given data,

performing a first set of logical operations on the first input data to generate a first output data, the first set of logical operations embodying a given input-output function,

performing a second set of logical operations on the second input data to generate a second output data, the second set of logical operations being different than the first set of logical operations and the second set of logical operations embodying the same given input-output function, and merging the first output data and the second output data to generate the cryptographic data output;

repeating said generating a mode signal to have a different one of the given plurality of states; and

repeating said receiving a given input data and generating a cryptographic processed data output.

17. (New) The electronic circuit of claim 1,

wherein the first combinatorial logical circuit comprises a first configuration of logical gates receiving a given power supply current, having an input, arranged to receive an input data *A* at said input and generate a cryptographic output data = *f*(A), *f* being a given function, by performing *f*(A) as a first set of logical operations on said first configuration of logical gates,

wherein said first configuration and said first set of logical operations are configured to generate a first power consumption profile when performing *f*(A), and

wherein the first combinatorial logical circuit comprises a second configuration of logical gates receiving a given power supply current, having an input, arranged to receive an input data *A* at said input and generate a cryptographic output data = *g*(A), *g* being a given function, wherein *g*(A) = *f*(A) for all A in a given range of A, by performing *g*(A) as a second set of logical operations on said second configuration of logical gates, and wherein said second configuration and said second set of logical operations are configured to generate a second power consumption profile when performing *g*(A) different from the first power consumption profile in performing *f*(A).

18. (New) The electronic circuit of claim 17,

wherein the selector is configured for receiving a given input data A and dynamically selecting from among the first combinatorial logical circuit for performing said *f*(A) = the cryptographic output data and the second combinatorial logical circuit for performing said *g*(A) = the cryptographic output data and producing a selected cryptographic output data as a selected on of either of *f*(A) and *g*(A), based said dynamic selecting.

19. (New) The electronic circuit of claim 1,

wherein the first combinatorial logical circuit comprises a first configuration of AND, OR and NOT logical gates receiving a given power supply current, having an input, arranged to receive an input data *A* at said input and generate a cryptographic output data = *f*(A), *f* being a given function, by performing *f* (A) as a first set of logical AND, OR and NOT operations on said first configuration of AND, OR and NOT logical gates, and

wherein the second combinatorial logical circuit comprises a second configuration of AND, OR and NOT logical gates receiving a given power supply current, having an input, arranged to receive an input data A at said input and generate a cryptographic output data = $g(A)$, g being a given function, wherein $g(A) = f(A)$ for all A in a given range of A, by performing $g(A)$as a second set of logical AND, OR and NOT operations on said second configuration of AND, OR and NOT logical gates, and

wherein said second configuration and said second set of logical AND, OR and NOT operations are different from said first configuration and said first set of logical AND, OR and NOT operations

20. (New) The electronic circuit of claim 19,

wherein the selector is configured to receive the given input data A and dynamically select from among the first combinatorial logical circuit for performing said $f(A)$ = the cryptographic output data and the second combinatorial logical circuit for performing said $g(A)$ = the cryptographic output data and to produce a selected cryptographic output data as a selected one of $f(A)$ and $g(A)$, based on said dynamic selecting.

21. (New) The electronic circuit of claim 20,

wherein the first combinatorial logical circuit comprises a first configuration of AND, OR and NOT logical gates receiving a given power supply current, having an input, arranged to receive an input data A at said input and generate a cryptographic output data = $f(A)$, f being a given function, by performing *f* (A)as a first set of logical AND, OR and NOT operations on said first configuration of AND, OR and NOT logical gates, wherein said first configuration and said first set of logical AND, OR and NOT operations are configured to generate a first power consumption profile when performing *f*(A), and

wherein the second combinatorial logical circuit comprises a second combinatorial logical circuit comprising a second configuration of AND, OR and NOT logical gates receiving a given power supply current, having an input, arranged to receive an input data *A* at said input and generate a cryptographic output data = *g*(A), *g* being a given function, wherein *g*(A) = *f*(A) for all A in a given range of A, by performing *g*(A)as a second set of logical AND, OR and NOT operations on said second configuration of AND, OR and NOT logical gates, and

wherein said second configuration and said second set of logical AND, OR and NOT operations are different from said first configuration and said first set of logical AND, OR and NOT operations and wherein said second configuration and said second set of logical AND, OR and NOT operations are configured to generate a second power consumption profile when performing *g*(A) and, wherein, for a given A, the first power consumption profile in performing f(A) is different from the second power consumption profile in performing g(A).

22. (New) The electronic circuit of claim 2,

wherein the first combinatorial logical circuit comprises a first configuration of AND, OR and NOT logical gates receiving a given power supply current, having an input, arranged to receive an input data *A* at said input and generate a cryptographic output data = *f*(A), *f* being a given function, by performing *f* (A)as a first set of logical AND, OR and NOT operations on said first configuration of AND, OR and NOT logical gates, wherein said first configuration and said first set of logical AND, OR and NOT operations are configured to generate a first power consumption profile when performing *f*(A),

wherein the second combinatorial logical circuit comprises a second combinatorial logical circuit comprising a second configuration of AND, OR and NOT logical gates receiving a given power supply current, having an input, arranged to receive an input data *A* at said input and generate a cryptographic output data = *g*(A), *g* being a given function, wherein *g*(A) = *f*(A) for all A in a given range of A, by performing *g*(A)as a second set of logical AND, OR and NOT operations on said second configuration of AND, OR and NOT logical gates, and

wherein said second configuration and said second set of logical AND, OR and NOT operations are different from said first configuration and said first set of logical AND, OR and NOT operations,

wherein said second configuration and said second set of logical AND, OR and NOT operations are configured to generate a second power consumption profile when performing *g*(A) and, wherein, for a given A, the first power consumption profile in performing f(A) is different from the second power consumption profile in performing g(A),

wherein the third combinatorial logical circuit comprises a third configuration of AND, OR and NOT logical gates receiving a given power supply current, having an input, arranged to receive an input data *B* at said input and generate a cryptographic output data = *f1*(B), *f1* being a given function, by performing *f1* (B)as a third set of logical AND, OR and NOT operations on said third configuration of AND, OR and NOT logical gates,

wherein said third configuration and said third set of logical AND, OR and NOT operations are configured to generate a third power consumption profile when performing *f1*(A), and

a fourth combinatorial logical circuit comprising a fourth configuration of AND, OR and NOT logical gates receiving a given power supply current, having an input, arranged to receive an input data *B* at said input and generate a cryptographic output data ,

wherein said cryptographic output data = *g1*(B), *g1* being a given function, wherein *g1*(B) = *f1*(B) for all B in a given range of B, by performing *g1*(B) as a fourth set of logical AND, OR and NOT operations on said fourth configuration of AND, OR and NOT logical gates, wherein said fourth configuration and said fourth set of logical AND, OR and NOT operations are different from said third configuration and said third set of logical AND, OR and NOT operations,

wherein said fourth configuration and said fourth set of logical AND, OR and NOT operations are configured to generate a fourth power consumption profile when performing *g1*(B) and,

wherein, for a given B, the third power consumption profile in performing *f1*(B) is different from the fourth power consumption profile in performing *g1*(B).